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You can also enter a full question or concept in plain language.

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- Capitalize proper nouns to search for specific people, places, or products.

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- Enclose a phrase in double quotes to search for that exact phrase.

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Article Information

View: 1-3 | [View](#)**1. A 33 GB/s 13.4 Mb integrated graphics accelerator and frame buffer**

Torrance, R.; Mes, I.; Hold, B.; Jones, D.; Crepeau, J.; DeMone, P.; MacDonald, D.; O'Connell, P.; White, R.; Duggins, S.; Fielder, D.  
Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE Int'l 5-7 Feb 1998

Page(s): 340-341, 461

**Summary:** Reported integrated DRAM and logic devices separate DRAM and ASIC logic port to traditional memory interface. Although this approach has a number of benefits over the discrete greater improvements are available by more tightly .....

[AbstractPlus](#) | Full Text: [PDF](#) IEEE CNF**2. An SDRAM interface for simplified "at-speed" testing of the SDRAM internal array**

Wu, J.; Paris, L.; Stender, J.; Harrison, I.; DeMone, P.; Millar, B.; Benzreba, J.; Gillingham, P.  
Memory Technology, Design and Testing, 1998. Proceedings. International Workshop on 24-25 Aug 1998

Page(s): 38-44

**Summary:** This paper outlines the SDRAM interface and the functional architecture of a first generation SDRAM device. We also discuss the means of testing and characterizing the DRAM array with using high speed testers for the entire test and.....

[AbstractPlus](#) | Full Text: [PDF](#) IEEE CNF**3. A 6.25 ns random access 0.25  $\mu$ m embedded DRAM**

DeMone, P.; Dunn, M.; Haerle, D.; Jin-Ki Kim; Macdonald, D.; Nyasulu, P.; Perry, D.; Smith, S.; Zhouhong Zhang  
VLSI Circuits, 2001. Digest of Technical Papers. 2001 Symposium on 2001

Page(s): 237-240

**Summary:** A new embedded DRAM architecture with uniform low latency operation was developed for computing, signal processing, and networking applications. Two hard macro blocks 104 K $\times$ 24b were implemented in a 0.25 micron stacked capacitor.....

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